AMENDMENTS TO THE CLAIMS

Listing of Claims

1. (Currently Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming an etch stop layer having a multi-layer structure along a profile containing conductive patterns formed on a substrate;

etching selectively a first inter-layer insulation layer deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns;

forming a first plug by depositing a conductive layer on an entire surface of [[the]] a resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns;

performing a cleaning process to remove remnants from the planarizing process;

forming an attack barrier layer on an entire surface of a resulting structure, wherein the attack barrier layer removes a plurality of gaps in the etch stop layer which occur during the planarizing process and the cleaning process;

forming a second inter-layer insulation layer;

etching selectively the second inter-layer insulation layer deposited along a profile containing the first plug to form a second contact hole exposing the first plug;

~~forming an attack barrier layer above the etch stop layer exposed by the second contact hole wherein the attack barrier layer removes a gap formed when the second contact hole is formed~~; and

forming a second plug electrically connected to the first plug through the second contact hole.

2. (Original) The method as recited in claim 1, wherein the multi-layer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating

material-based layer being disposed between the nitride layers -and having a lower dielectric constant than those of the nitride layers

3. (Previously Presented) The method as recited in claim 1, wherein the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole.

4. (Original) The method as recited in claim 3, wherein in etching the partial portion of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern, the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern ranges from about 500 Angstroms to about 1500 Angstroms.

5. (Original) The method as recited in claim 1, wherein after the step of performing the cleaning process, the attack barrier layer is deposited on an entire surface of the profile containing the first plug.

6. (Original) The method as recited in claim 1, wherein after the step of forming the second contact hole, the attack barrier layer is formed along a profile containing the second contact hole.

7. (Original) The method as recited in claim 1, wherein the attack barrier layer is a nitride-based layer.

8. (Original) The method as recited in claim 1, wherein the attack barrier layer has a thickness ranging from about 50 Angstroms to about 500 Angstroms.

9. (Original) The method as recited in claim 2, wherein the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_2O_3) layer and a tantalum oxynitride (TaON) layer.

10. (Original) The method as recited in claim 1, wherein the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE).

11. (Original) The method as recited in claim 1, wherein the conductive pattern is a gate electrode pattern and the second plug is a storage node contact plug.

12. (Currently Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming an etch stop layer having a multi-layer structure along a profile containing conductive patterns formed on a substrate;

etching selectively a first inter-layer insulation layer deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns;

forming a first plug by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns;

performing a cleaning process to remove remnants from the planarizing process;

forming an attack barrier layer on an entire surface of [[the]] <u>a</u> resulting structure including the first plug<u>, the conductive patterns, and the etch stop layer, wherein the attack barrier layer removes a plurality of gaps which occur during the planarizing process and the cleaning process</u>;

<u>forming a second inter-layer insulation layer;</u>

etching selectively the second inter-layer insulation layer formed on the attack barrier layer and the attack barrier layer to form a second contact hole exposing the first plug; and

forming a second plug electrically connected to the first plug through the second contact hole~~; wherein an attack barrier layer formed between the second plug and the conductive patterns removes a gap formed when the second contact hole is formed~~.

13. (Original) The method as recited in claim 12, wherein the multi-layer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layers and having a lower dielectric constant than those of the nitride layers.

14. (Previously Presented) The method as recited in claim 12, wherein the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole.

15. (Original) The method as recited in claim 14, wherein in case of etching the partial portion of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern, the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern preferably ranges from about 500 Angstrom to about 1500 Angstrom.

16. (Original) The method as recited in claim 12, wherein the attack barrier layer is a nitride-based layer.

17. (Original) The method as recited in claim 12, wherein the attack barrier layer has a thickness ranging from about 50 Angstrom to about 500 Angstrom.

18. (Original) The method as recited in claim 13, wherein the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an Al_2O_3 layer and a TaON layer.

19. (Original) The method as recited in claim 12, wherein the cleaning process uses a cleaning solution of HF or BOE.

20. (Original) The method as recited in claim 12, wherein the conductive pattern is a gate electrode pattern and the second plug is a storage node contact plug.

21-30. (Canceled)

31. (Previously Presented) The method as recited in claim 1, wherein the second inter-layer insulation layer has a flow-fill property.

32. (Original) The method as recited in claim 31, wherein the second inter-layer insulation layer is made of an oxide-based material selected from a group consisting of advanced planarization layer (APL), spin on dielectric (SOD), spin on glass (SOG) and borophosphosilicate glass (BPSG).

33-35. (Canceled)

36. (Original) The method as recited in claim 31, wherein the second inter-layer insulation layer has a thickness ranging from about 1000 Angstrom to about 8000 Angstrom.

37-39. (Canceled)